Characterization of Graphene Films and Transistors Grown on Sapphire by Metal-Free Chemical Vapor Deposition

Mark A. Fanton,[†,*] Joshua A. Robinson,[†,‡,*] Conor Puls,[§] Ying Liu,[§] Matthew J. Hollander,[‡] Brian E. Weiland,[†] Michael LaBella,[†] Kathleen Trumbull,[†] Richard Kasarda,[†] Casey Howsare,[†,‡] Joseph Stitt,[⊥] and David W. Snyder[†,#]

[†]The Electro-Optics Center, [‡]Department of Materials Science and Engineering, [§]Department of Physics, [⊥]Materials Research Institute [#]Department of Chemical Engineering, The Pennsylvania State University, University Park, Pennsylvania 16802, United States

ABSTRACT We present a novel method for the direct metal-free growth of graphene on sapphire that yields high quality films comparable to that of graphene grown on SiC by sublimation. Graphene is synthesized on sapphire *via* the simple decomposition of methane at 1425−1600 °C. Film quality was found to be a strong function of growth temperature. The thickness, structure, interface characteristics, and electrical transport properties were characterized in order to understand the utility of this material for electronic devices. Graphene synthesized on sapphire is found to be strain relieved, with no evidence of an interfacial buffer layer. There is a strong correlation between the graphene structural quality and carrier mobility. Room temperature Hall effect mobility values were as high as 3000 $cm^2/(V\,s)$, while measurements at 2 K reached values of 10 500 $cm^2/(V\,s)$. These films also display evidence of the quantum Hall effect. Field effect transistors fabricated from this material had a typical current density of 200 mA/mm and transconductance of 40 mS/mm indicating that material performance may be comparable to graphene on SiC.

KEYWORDS: graphene · chemical vapor deposition · sapphire · mobility · Hall effect

Recent success of graphene transistor operation in the GHz frequency range demonstrates the potential of this material for high speed electronics.[1−3] The most promising route for large area, electronic grade graphene is synthesis *via* sublimation of Si from the surface of single crystal SiC semiconductor wafers.[4] While this technique has achieved carrier mobilities greater than 18 000 $cm^2/(V\,s)$ at room temperature on SiC(000$\bar{1}$), controlling the graphene thickness on SiC(000$\bar{1}$) can be quite challenging.[5] Alternatively, monolayer graphene is readily achieved on SiC (0001), but the formation of a "buffer layer" between graphene and SiC(0001) results in a 10× reduction in mobility. As a result, methods such as spin deposition of reduced graphene oxide,[6] dry transfer from SiC,[7] chemical vapor deposition (CVD) on metal substrates,[8,9] and plasma-assisted deposition[10] have been explored as a means to achieve ultralarge area, high mobility graphene. Of these techniques, CVD is likely the most attractive alternative to silicon sublimation from SiC due to the inherent control over process chemistry and the flexibility in choosing precursors. CVD is an established method for the production carbon-based materials including pyrolytic graphite,[11] carbon/carbon composites,[12] diamond,[12] and carbon nanotubes.[13] Additionally, CVD has been utilized to form graphene on Ni[14] or Cu[9] at temperatures near 1000 °C. However, the presence of a metal substrate induces its own challenges for the production of semiconductor devices. As a result, there is a desire to produce high quality graphene films without a metallic catalyst. Ismach *et al.*[15] report chemical vapor deposition of graphene on sapphire *via* the use of a thin sacrificial Cu film that evaporates during graphene synthesis. While this process yields high quality graphene, the film is discontinuous and is thus difficult to utilize in standard CMOS processing. Alternatively, Maeda and Hibino[16] have shown that deposition of thin carbon films on sapphire and Si without a metal catalyst is possible using gas source molecular beam epitaxy (MBE). This process yields continuous films, but utilizes deposition temperatures near 600 °C, which produce low quality films as characterized by Raman spectroscopy. Most recently, Hwang *et al.*[17] demonstrated metal-free growth of graphitic films on sapphire and SiC at temperatures of 1350−1650 °C. They provided evidence that the film structure is ABC-stacked, and that film quality improved with deposition temperature. In fact, Raman spectroscopy of these films exhibited D-peak to G-peak ratios as low as 0.06, suggesting that the structural quality may be comparable to that of graphene on silicon carbide. However, the reported film thickness (nine monolayers on sapphire and four

* Address correspondence to mfanton@psu.edu, jrobinson@psu.edu.

Received for review July 14, 2011 and accepted September 9, 2011.

Published online September 11, 2011
10.1021/nn202643t

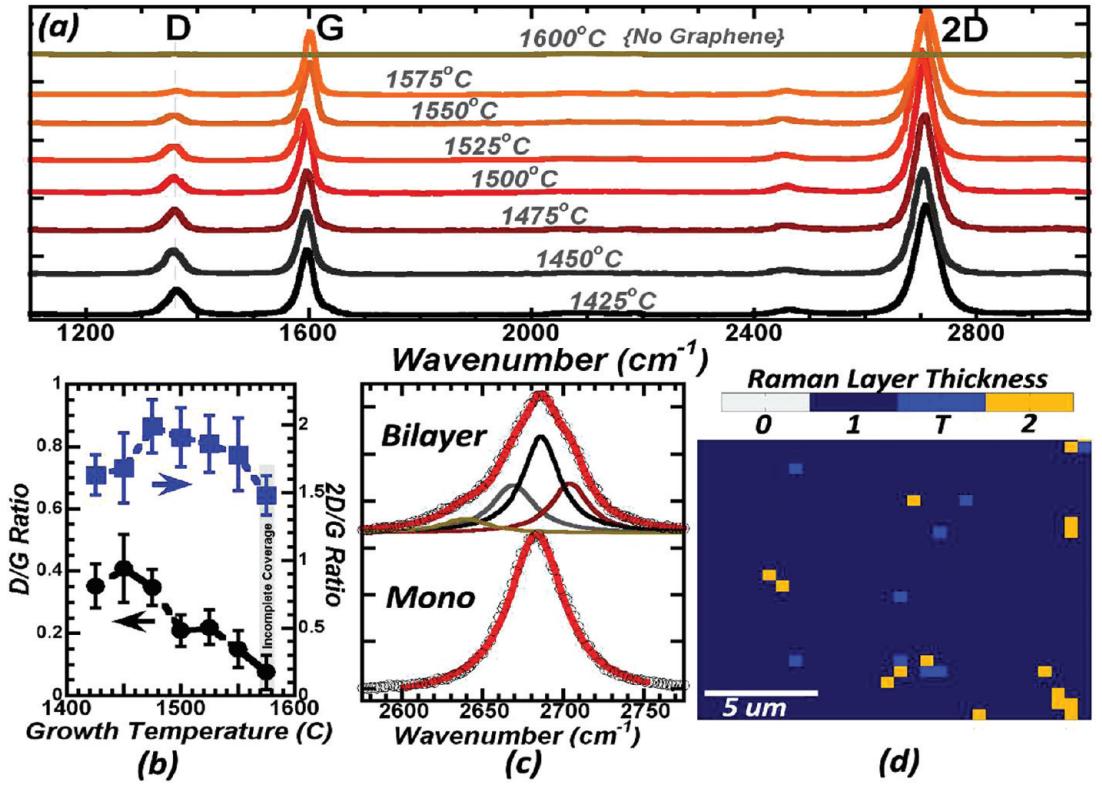

Figure 1. (a) Raman spectroscopy of graphene on sapphire indicates that structural quality improves as the growth temperature is increased from 1425 to 1575 °C. Additionally, the 2D/G ratio (b) remains equal to or greater than 1.5 with a significant fraction of the 2D Raman spectra being fit to one or four Lorentzian curves (c) suggesting the presence of monolayer and bilayer graphene. Finally, Raman mapping and subsequent peak fitting of the 2D peak for a film grown at 1525 °C indicates >90% monolayer coverage (d).

monolayers on SiC(000$\bar{1}$)) precludes the use of this material in electronic devices where current modulation is required.

RESULTS AND DISCUSSION

We present a CVD process for growth of high quality monolayer graphene on sapphire with D/G ratios as low as 0.05, long-range roughness <1 nm, and carrier mobilities exceeding 3000 $cm^2/(V\ s)$ over 50 mm diameter substrates. Additionally, we examine the graphene/Al_2O_3 system to correlate growth conditions with structural, chemical, and electronic properties to show a clear trend with process temperature. This process provides a means for scale-up to low cost, large diameter substrates and yields material performance paralleling that of epitaxial graphene on the Si-face of SiC, which is the current leader for large scale fabrication of high frequency analog devices.[1,2]

Prior to the growth of graphene on sapphire, it is important to evaluate the thermodynamic equilibrium conditions of the Al−C−O−H chemical system to determine appropriate boundary conditions for solid C deposition and to determine the thermodynamically stable reaction products. Thermo-chemical modeling was accomplished *via* free energy minimization using HSC Chemistry 5.11. While this analysis is not quantitative in nature, it does provide valuable insight into the trends expected when attempting to deposit solid C at various temperatures, pressures, and reactant concentrations. In the case of graphene synthesis on sapphire substrates (1450−1700 °C), the potential for reaction between C and sapphire (Al_2O_3) is the primary concern. Modeling of a system composed of Al, O, C, H, and Ar predicts that no solid phase Al−C or O−C containing products will form, suggesting that no covalent bonding will occur between the graphene film and substrate. However, both CO(g) and Al_2O(g) are predicted to be present in significant concentrations above 1200 °C, and may completely consume all of the CH_4 above 1400 °C. This indicates that two undesirable effects may take place during CVD of graphene on sapphire. The first is that no solid carbon will exist if the reaction to form CO(g) proceeds at a rate significantly faster than the rate of CH_4 decomposition to solid C. The second is that the presence of C in either solid or gaseous forms may significantly etch the surface of the sapphire substrate making it too rough for semiconductor device processing. Experimental observations showed that prior to growth, and up to growth temperatures of 1500 °C, the average roughness (R_a) of the sapphire substrates was 0.3−0.5 nm when using a typical CH_4 concentration of 0.5% in the growth atmosphere. Also, when heated up to 1550 °C in a 10% H_2/Ar ambient, with no CH_4 present, there was

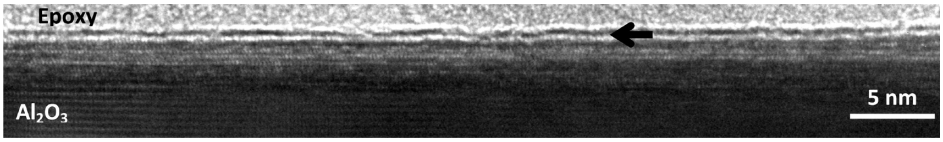

Figure 2. High resolution transmission electron microscope image of the cross section of a graphene film deposited on a sapphire substrate by CVD.

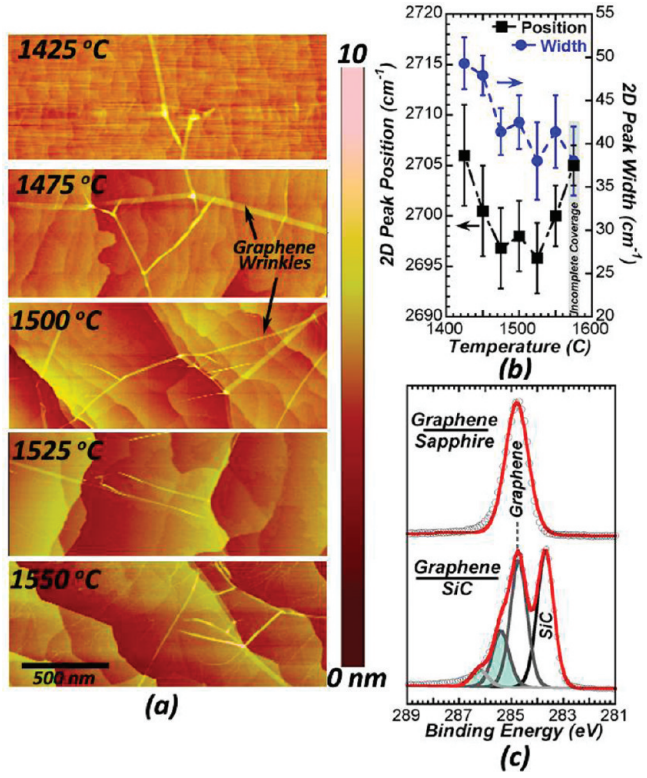

Figure 3. Atomic force microscopy (a) indicates the presence of wrinkles in the graphene on sapphire, which serve as a strain relief mechanism as indicated by Raman spectroscopy (b), where the peak position of the 2D peak indicates <0.1% strain. Additionally, Raman (b) and XPS (c) indicate little interaction between graphene and sapphire, with no indication of an interfacial (buffer) layer. Note: Sapphire XPS spectra are charge referenced to the Al 2p peak at 74.5 eV.

no measurable change in surface roughness. However, with 0.5% CH_4 added to the gas mixture the surface roughness increased to 2.9 nm at 1525 °C, then to 6.3 nm at 1550 °C, with a high density of hexagonal etch pits. This indicates that the addition of C to the growth environment was responsible for etching the surface.

Raman spectroscopy was used extensively to characterize the C films grown on sapphire. The graphene D-peak (1360 cm^{-1}) to G-peak (~1590 cm^{-1}) ratio has been used extensively to characterize the structural quality (domain size) of graphene films.[18] Raman spectroscopy confirms the formation of thin carbon layers on sapphire, at deposition times of 30 s or more. There appears to be a short induction period before growth begins similar to that observed by Hwang *et al.*[17] For the shortest growth times, using the D/G ratio, we find that the domain size increases from an average low of 32 nm at 1425−1450 °C (D/G = 0.42) to greater than 270 nm (D/G = 0.05) at 1575 °C (Figure 1a,b). Additionally, we find that in all cases, the 2D/G ratio is greater than 1.5 with the 2D peak being fit to either one or four Lorentzians, suggesting deposition of mono- or multilayer graphene (Figure 1b,c) is achieved. For growth times exceeding 45 s the 2D/G ratio rapidly dropped below 1 indicating growth of multilayer films.

The 2D peak width correlates well with the D/G ratio, and may be used as a measure of the relative quality of the graphene material. As the growth temperature increases, we find that the 2D peak width decreases from a high of 50 to 35 cm^{-1} (Figure 3b), indicating improvement in the graphene structural quality akin to that of graphene on SiC. Interestingly, we find >90% of the Raman 2D-peak spectra, regardless of growth temperature, is fit to a single Lorentzian curve. Figure 1d is a 15 × 12.5 μm Raman map of the 2D peak for a film grown at 1525 °C that has been fit to Lorentzian curves to identify the "Raman" layer thickness. Each pixel in the map is colored to represent one of three categories of fit. Clearly evident is the dominant coverage of monolayer graphene (1), which is fit

to a single Lorentzian. In some cases we find regions with multilayer graphene (2), which is fit to four Lorentzians. Additionally, we find "transition" regions (T) where the Raman laser overlaps multiple domains and thus does not fit well to one or four Lorentzians. Finally, while we find improved structural quality as growth temperature increases Raman spectroscopy indicates only partial coverage (<20%) at 1575 °C, with no graphene formation above 1575 °C. This phenomenon is correlated with the significant increase in average surface roughness, indicating that etching of sapphire by C species occurs at a higher rate than graphene can be deposited.

High resolution transmission electron microscopy (HRTEM) confirms the presence of 1−2 layers of graphene on the sapphire surface. Figure 2 shows a cross section image of the sapphire/graphene interface with a distinct layer of graphene, noted by the arrow, which is very similar to the graphene observed on the Si-face of SiC substrates.[19] Absolute interpretation of the image as either one layer or two is not possible as the contrast is related to many factors including sample thickness, composition, structure, and imaging conditions.

In addition to structural quality the chemical nature of the interface between the graphene and the sapphire was examined. Strain in epitaxial graphene on SiC is the result of the formation of a covalently bound interfacial layer (buffer layer) that attaches the graphene and SiC substrate. This results in significant compressive strain in the graphene following sample cool down due to a difference in coefficients of thermal expansion (CTE) of graphene and SiC.[20] For monolayer graphene, it has been found that the 2D peak shifts from ~2685 cm^{-1} for exfoliated graphene to as high as 2760 cm^{-1} for monolayer epitaxial graphene on SiC.[21] In the case of graphene on sapphire the CTE difference is nearly double that of graphene on SiC,[22,23] suggesting that significantly more strain must be accommodated by the graphene film upon cooling to room temperature if the film is bound tightly to the sapphire surface. Similar to graphene on SiC(000$\bar{1}$), graphene films on sapphire exhibit wrinkling (Figure 3a), which likely serve as a mechanism for strain relief during cool down. However, we find that the wrinkles exhibit heights of only 0.4−1.5 nm, significantly smaller than those found on graphene grown on SiC(000$\bar{1}$).[24] Figure 3a summarizes the surface topography of the sapphire substrate, as well as the density of graphene winkles on sapphire. It is evident from Figure 3a that the density of wrinkles increases with the growth temperature. The reason for this may be related to several factors. First, the increased growth temperature would require an additional accommodation of the CTE differences upon cooling. Second, higher growth temperatures may create more attachment points between the film and the substrate either through chemical bonding or through increased mechanical coupling caused by the increased surface roughness at higher temperatures.

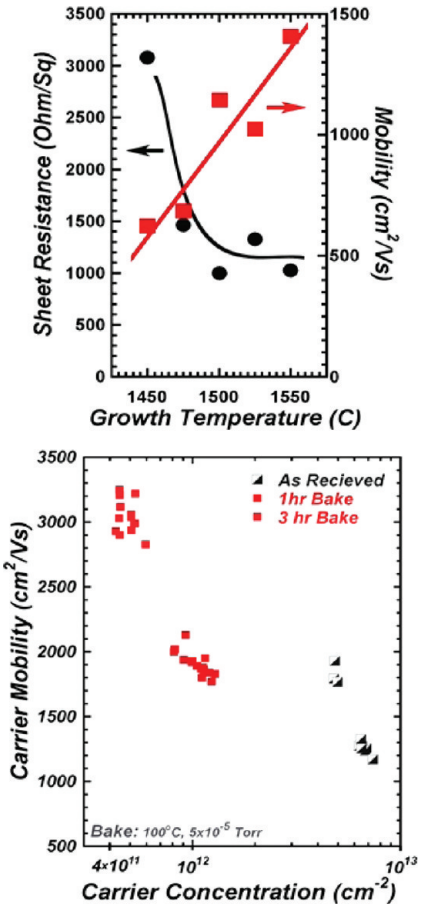

Figure 4. (a) Hall mobility and sheet resistance strongly correlates with CVD growth temperature. As growth temperature is increased, sheet resistance is reduced, while mobility improves by ~3×. (b) The Hall effect mobility increases significantly upon removal of adsorbed contaminants. In all cases the material remains n-type.

Raman spectroscopy (Figure 3b) confirms that little strain remains in the graphene film after cool down, as the 2D peak position ranges from 2685−2705 cm^{-1}, indicating minimal interaction between the graphene and sapphire. While we note the presence of a minimum in the peak position, indicating a temperature range over which strain relief is maximized, the mechanism for this phenomenon is not well understood and is currently under investigation.

To examine the chemical bonding between the substrate and the film, we employed XPS to evaluate Al−O−C bonding at the graphene/sapphire interface compared to graphene on SiC(0001). The formation of a buffer layer in graphene on SiC is well correlated with the presence of additional peaks in the carbon 1s spectra (Figure 3c).[25] In the case of sapphire, additional peaks from the Al−O−C interaction would be present if a significant interfacial layer were to exist. However, it is clear from the C 1s spectra (Figure 3c) that there are

nondetectable concentrations of Al−C bonds (281.5 eV) and Al−O−C bonds (282.5 eV) present at the interface.[26,27] As a result, we find no evidence of an interfacial (buffer) layer between graphene and sapphire, confirming results from thermodynamic modeling. However, the presence of the wrinkles in the graphene film does suggest there is some amount of mechanical coupling between the film and the substrate, although XPS indicates it is not primarily through chemical bonds.

Finally, carrier transport measurements confirm the formation of high quality graphene. As noted in Figure 4a, the sheet resistance decreases as a function of growth temperature and is correlated with an increase in carrier mobility. The decrease in sheet resistance is correlated with an increased layer thickness in epitaxial graphene on SiC; however, in the case of graphene on sapphire we find no evidence of increased thickness for the short growth times used in this work. As a result, we speculate that the improved sheet resistance (and carrier mobility) is linked to the improved structural quality and thus less charge carrier scattering in the film. As the D/G ratio decreases with increasing temperature, we find the carrier mobility increases from 600 $cm^2/(V\ s)$ (D/G = 0.4) to a high of 1400 $cm^2/(V\ s)$ (D/G = 0.1). Additionally, mobility and sheet resistance is evaluated at room temperature in ambient atmosphere using a noncontact Lehighton probe.[28] Lehighton probe measurements are completed at ambient room temperature and atmosphere, which leads to absorption of water vapor, as well as other environmental contaminants that may result in carrier scattering. As a result, 5 × 5 μm Van der Pauw structures are fabricated from graphene films grown at 1500 °C (approximately 1250 $cm^2/(V\ s)$ measured *via* Lehighton, Figure 4a) for Hall effect measurements under vacuum. Samples are annealed *in situ* at 1 × 10^{-8} Torr and 400 K before measurement in order to ensure desorption of water or other contaminants from the surface of the graphene, preventing any extrinsic doping or scattering in the graphene. Figure 4b clearly indicates that the presence of adsorbed molecules can significantly affect carrier mobility where we find that moderate annealing for 60 min reduces carrier concentration by 8 times and increases carrier mobility by 45% to 1800 $cm^2/(V\ s)$. Increasing the annealing time to 180 min results in a 94% reduction in carrier concentration (4.5 × 10^{11} cm^{-2}) and 240% increase in carrier concentration to an average value of 3000 $cm^2/(V\ s)$. In all cases the material exhibits n-type characteristics.

Additional electronic transport measurements of van der Pauw structures were carried out at low temperatures and magnetic fields up to 9 T. Devices were heated at 400 K and vacuum pumped to ~0.2 Torr for 1 h and maintained in vacuum during cooling to 2 K. Measurements of longitudinal resistance and

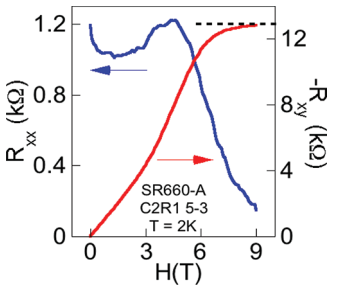

Figure 5. Hall resistances as a function of magnetic field for graphene on sapphire van der Pauw structures.

low field ($|H| < 2$ T) Hall coefficient in multiple devices suggest Hall mobilities reach as high as 10 500 $cm^2/(V\ s)$, while higher magnetic fields yield nonconstant Hall coefficients due to the emergence of quantum transport phenomena in the graphene films.

High film quality allows us to observe such quantum phenomena as the half-integer quantum Hall effect, unique to the Dirac cone band structure of single layer graphene, with low-temperature measurements of some van der Pauw structures. In graphene films with low disorder, high magnetic fields quantize the Hall resistance according to $R_{xy}^{-1} = 4(n + {}^1/_2)e^2/h$, where e is the elementary charge, h is Planck's constant, and n is an integer, an effect observed previously in graphene flakes mechanically exfoliated from bulk graphite.[29,30] In the device in Figure 5 the low field ($H < 2.5$T) Hall coefficient implies a carrier density $n_e \approx 4.53 \times 10^{11}$ electrons/cm^2 so that determining the Landau level carrier filling by $n_{LL} = 4H/\phi_0$ (where $\phi_0 = e/h$ is the magnetic flux quantum), a field $H = 9.4$ T would half-fill the zero-energy ($n = 0$) Landau level and quantize the Hall resistance to 12.9 kΩ. Up to our maximum applicable field of 9 T, measurements of the Hall resistance show that a plateau emerges at that expected quantization concurrent with the expected vanishing longitudinal resistance R_{xx} in the same device, both confirming single layer uniformity in the grown film.

Field effect transistors (FETs) were also fabricated from graphene films on sapphire using 10 nm thick HfO_2 gate dielectric deposited by a combined physical vapor deposition and atomic layer deposition technique.[31] The FETs are double finger structures with each finger having a gate length of 1.5 μm and a gate width of 3 μm. Transfer characteristics of FETs fabricated on 50 mm diameter wafers are characterized using an automated probing tool in order to map the device performance across the surface of the wafer. Figure 6a shows transfer curves of both typical and high quality devices exhibiting the ambipolar behavior characteristic of graphene. Devices displaying both p-type and n-type behavior were distributed across the test wafer in roughly equal proportions with no obvious groupings by location. Figure 6b is a map of the maximum drain−source current (I_{ds}) observed across the wafer with typical values of 100−200 mA/mm and the

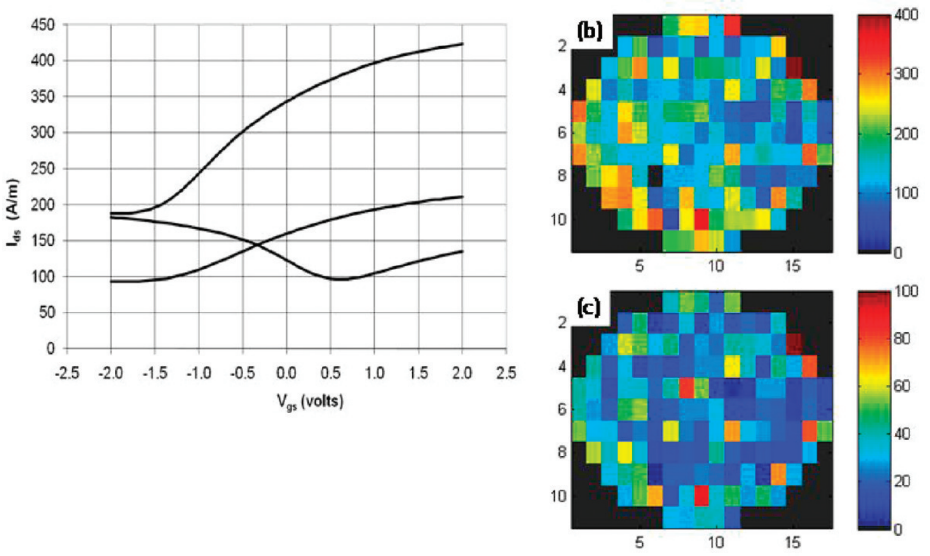

Figure 6. (a) Measured transfer characteristics of average and best case FETs taken from the 50 mm wafer maps of (b) maximum I_{ds} in mA/mm and (c) maximum g_m in mS/mm at a source-drain bias of 1 V.

best observed value of 400 mA/mm. Maximum transconductance (g_m) was also mapped across the wafer and ranges from 20 to 60 mS/mm as shown in Figure 6c. These values compare favorably with early graphene on SiC FETs which exhibited maximum I_{ds} and g_m values of 200 mA/mm and 98 mS/mm, respectively, using a similar device geometry and test conditions.[1] Top-gated graphene FETs fabricated on 3C-SiC on Si using a more optimized device design have displayed maximum I_{ds} and g_m values of 225 mA/mm and 40 mS/mm, respectively.[32] Comparing the performance to graphene grown catalytically on Ni by CVD and then transferred to an insulating substrate is also instructive. This material has similar structural characteristics based on Raman spectroscopy[33] and yields similar transport characteristics with maximum I_{ds} values ranging from 40 to 150 mA/mm and g_m values ranging from 15 to 75 mS/mm.[34]

CONCLUSIONS

We have presented a novel method for the direct deposition of graphene on an insulating substrate that may be an attractive alternative to graphene formed on SiC by sublimation. This deposition technique results in high structural quality graphene with D/G ratios as low as 0.05 and essentially no covalent bonding between the substrate and the film. While the structural quality and carrier mobility are comparable to graphene on SiC(0001), it remains below that of exfoliated graphene despite the significant strain relief. The reduction in carrier mobility compared to exfoliated graphene is likely tied to the presence of defects in the material (D-peak is still present), and to a lesser extent any remaining graphene/sapphire interaction as noted by the small presence of strain in the graphene. The performance of graphene/sapphire FETs is expected to improve as the structural quality and the uniformity of the material improves. Further improvement of the graphene is expected through tailoring the initial stages of graphene synthesis. Very little is understood about growth initiation on sapphire and the interdependencies between gas phase chemistry, carbon deposition, and competing reactions with the sapphire surface.

MATERIALS AND METHODS

Synthesis of Graphene Films. Graphene films were deposited on standard 50 mm diameter c-plane sapphire wafers (Crystal Systems, Inc.) in a commercial high-temperature semiconductor CVD tool (Structured Materials, Inc.). Prior to growth the substrates were cleaned with Baker Clean Solution 111 (JT Baker) for 15 min at 60 °C and then rinsed with 18 MΩ water followed by acetone and isopropyl alcohol. Films were synthesized from the decomposition of a mixture of 10% methane (CH_4) in hydrogen (H_2) in an argon (Ar) carrier gas. Typical CH_4 concentration in the growth atmosphere was 1.5 vol %. Growths were performed at 1425−1700 °C at pressures of 50−600 Torr. Upon reaching the specified growth temperature, graphene synthesis was carried out for times ranging from 30 s to 20 min, after which the carbon source was shut off and the sample was returned to room temperature under Ar ambient.

Device Fabrication. Test structures and transistors are fabricated using standard UV photolithography techniques. Van der Pauw (VdP) structures for Hall effect measurements are 5 × 5 μm squares, while transistors utilize two-finger gates 2 × (3 × 1.5) μm ($W \times L$) with 1 μm source−drain spacing. Source/drain contacts (Ti/Au 10/50 nm) are prepared using an oxygen plasma pretreatment.[35] Dielectric deposition is accomplished *via* a two step process that includes direct deposition of a HfO_2 seed layer *via* e-beam evaporation followed by atomic layer deposition of 8 nm HfO_2 in a Cambridge Nanotech, Inc. "Savannah"

ALD system. Finally, gate metallization was completed *via* UV lithography and deposition of a Ti/Au metal stack.

Characterization. Sample surfaces were characterized *via* white light interferometry, optical microscopy (OM), and atomic force microscopy (AFM). Film and interfacial bond chemistry was evaluated *via* X-ray photoelectron spectroscopy (XPS). Additionally, graphene films were characterized *via* Raman spectroscopy (WiTec, 488 nm laser) to assess the structural quality (D/G ratio),[18] thickness (peak fitting of 2D peak),[36] and strain (2D peak position, post thickness verification).[20,21] Carrier mobility measurements were acquired at room temperature after a bake out at 200 °C using a Nanometrics HL5500 Hall Effect measurement tool. Transistor transfer curves were collected using a Kiethley 4200-SCS (Semiconductor Characterization System) in conjunction with Kiethley ACS (Automated Characterization Suite) software and Cascade Summit 10000 Semiautomatic Probe Station for fully automatic, wafer-scale data acquisition. All $I_{ds}-V_{gs}$ sweeps were collected with $V_{ds} = 1$ V and V_{gs} swept between -2 to $+2$ V. Wafer maps were created by plotting the results of single transistor measurements within each 2.5 $\times$ 4.5 mm die across the surface of the wafer.

Acknowledgment. This work was supported by the Naval Surface Warfare Center Crane, Contract No. N00164-09-C-GR34. Additionally, support for the WiteC Raman, Kratos XPS, Jeol TEM, and the Penn State Nanofabrication Facility was provided in part by the National Nanotechnology Infrastructure Network at Penn State.

REFERENCES AND NOTES

1. Moon, J. S.; Curtis, D.; Hu, M.; Wong, D.; McGuire, C.; Campbell, P. M.; Jernigan, G.; Tedesco, J. L.; VanMil, B.; Myers-Ward, R.; Eddy, C.; *et al*. Epitaxial-Graphene RF Field-Effect Transistors on Si-Face 6H-SiC Substrates. *IEEE Elect. Dev. Lett.* **2009**, *30*, 650–652.
2. Lin, Y. M.; Dimitrakopoulos, C.; Jenkins, K. A.; Farmer, D. B.; Chiu, H. Y.; Grill, A.; Avouris, P. 100-GHz Transistors from Wafer-Scale Epitaxial Graphene. *Science* **2010**, *327*, 662–662.
3. Liao, L.; Bai, J. W.; Cheng, R.; Lin, Y. C.; Jiang, S.; Qu, Y. Q.; Huang, Y.; Duan, X. F. Sub-100 nm Channel Length Graphene Transistors. *Nano Lett.* **2010**, *10*, 3952–3956.
4. Berger, C.; Song, Z. M.; Li, X. B.; Wu, X. S.; Brown, N.; Naud, C.; Mayou, D.; Li, T. B.; Hass, J.; Marchenkov, A. N.; Conrad; *et al*. Electronic Confinement and Coherence in Patterned Epitaxial Graphene. *Science* **2006**, *312*, 1191–1196.
5. Robinson, J. A.; Wetherington, M.; Tedesco, J. L.; Campbell, P. M.; Weng, X.; Stitt, J.; Fanton, M. A.; Frantz, E.; Snyder, D.; VanMil; *et al*. Correlating Raman Spectral Signatures with Carrier Mobility in Epitaxial Graphene: A Guide to Achieving High Mobility on the Wafer Scale. *Nano Lett.* **2009**, *9*, 2873–2876.
6. Stankovich, S.; Dikin, D. A.; Piner, R. D.; Kohlhaas, K. A.; Kleinhammes, A.; Jia, Y.; Wu, Y.; Nguyen, S. T.; Ruoff, R. S. Synthesis of Graphene-Based Nanosheets *via* Chemical Reduction of Exfoliated Graphite Oxide. *Carbon* **2007**, *45*, 1558–1565.
7. Caldwell, J. D.; Anderson, T. J.; Culbertson, J. C.; Jernigan, G. G.; Hobart, K. D.; Kub, F. J.; Tadjer, M. J.; Tedesco, J. L.; Hite, J. K.; Mastro; *et al*. Technique for the Dry Transfer of Epitaxial Graphene onto Arbitrary Substrates. *ACS Nano* **2010**, *4*, 1108–1114.
8. Kim, K. S.; Zhao, Y.; Jang, H.; Lee, S. Y.; Kim, J. M.; Kim, K. S.; Ahn, J. H.; Kim, P.; Choi, J. Y.; Hong, B. H. Large-Scale Pattern Growth of Graphene Films for Stretchable Transparent Electrodes. *Nature* **2009**, *457*, 706–710.
9. Li, X.; Cai, W.; An, J.; Kim, S.; Nah, J.; Yang, D.; Piner, R.; Velamakanni, A.; Jung, I.; Tutuc, E.; Banerjee, S. K.; Colombo, L.; Ruoff, R. S. Large-Area Synthesis of High-Quality and Uniform Graphene Films on Copper Foils. *Science* **2009**, *324*, 1312–1314.
10. Malesevic, A.; Vitchev, R.; Schouteden, K.; Volodin, A.; Zhang, L.; Van Tendeloo, G.; Vanhulsel, A.; Van Haesendonck, C. Synthesis of Few-Layer Graphene *via* Microwave Plasma-Enhanced Chemical Vapour Deposition. *Nanotechnology* **2008**, *19*, 3056041–3056046.
11. Taylor, C. Characterization of CVD Carbon Films for Hermetic Optical Fiber Coatings. *Surf. Coat. Technol.* **2003**, *168*, 1–11.
12. Park, J.-H. *Chemical Vapor Deposition*; ASM International: Materials Park, OH, 2001.
13. Cassell, A. M.; Raymakers, J. A.; Kong, J.; Dai, H. J. Large Scale CVD Synthesis of Single-Walled Carbon Nanotubes. *J. Phys. Chem. B* **1999**, *103*, 6484–6492.
14. Reina, A.; Jia, X. T.; Ho, J.; Nezich, D.; Son, H. B.; Bulovic, V.; Dresselhaus, M. S.; Kong, J.; Area, Layer Few-Layer Graphene Films on Arbitrary Substrates by Chemical Vapor Deposition. *Nano Lett.* **2009**, *9*, 3087–3087.
15. Ismach, A.; Druzgalski, C.; Penwell, S.; Schwartzberg, A.; Zheng, M.; Javey, A.; Bokor, J.; Zhang, Y. Direct Chemical Vapor Deposition of Graphene on Dielectric Surfaces. *Nano Lett.* **2010**, *10*, 1542–1548.
16. Maeda, F.; Hibino, H. Thin Graphitic Structure Formation on Various Substrates by Gas-Source Molecular Beam Epitaxy Using Cracked Ethanol. *Jpn. J. Appl. Phys.* **2010**, *49*, 04DH13.
17. Hwang, J.; Shields, V. B.; Thomas, C. I.; Shivaraman, S.; Hao, D.; Kim, M.; Woll, A. R.; Tompa, G. S.; Spencer, M. G. Epitaxial Growth of Graphitic Carbon on C-face SiC and Sapphire by Chemical Vapor Deposition (CVD). *J. Cryst. Growth* **2010**, *312*, 3219–3224.
18. Cancado, L. G.; Takai, K.; Enoki, T.; Endo, M.; Kim, Y. A.; Mizusaki, H.; Jorio, A.; Coelho, L. N.; Magalhaes-Paniago, R.; Pimenta, M. A. General Equation for the Determination of the Crystallite Size of Nanographite by Raman Spectroscopy. *Appl. Phys. Lett.* **2006**, *88*, 163106-1–163106-3.
19. Robinson, J.; Weng, X. J.; Trumbull, K.; Cavalero, R.; Wetherington, M.; Frantz, E.; LaBella, M.; Hughes, Z.; Fanton, M.; Snyder, D. Nucleation of Epitaxial Graphene on SiC(0001). *ACS Nano* **2010**, *4*, 153–158.
20. Ferralis, N.; Maboudian, R.; Carraro, C. Evidence of Structural Strain in Epitaxial Graphene Layers on 6H-SiC(0001). *Phys. Rev. Lett.* **2008**, *101*, 156801-1–156801-4.
21. Robinson, J. A.; Puls, C. P.; Staley, N. E.; Stitt, J. P.; Fanton, M. A.; Emtsev, K. V.; Seyller, T.; Liu, Y. Raman Topography and Strain Uniformity of Large-Area Epitaxial Graphene. *Nano Lett.* **2009**, *9*, 964–968.
22. Prakash, G.; Capano, M. A.; Bolen, M. L.; Zemlyanov, D.; Reifenberger, R. G. AFM Study of Ridges in Few-Layer Epitaxial Graphene Grown on the Carbon-Face of 4H−SiC-(000$\bar{1}$). *Carbon* **2010**, *48*, 2383–2393.
23. Yim, W. M.; Paff, R. J. Thermal Expansion of AlN, Sapphire, and Silicon. *J. Appl. Phys.* **1974**, *45*, 1456–1457.
24. Tedesco, J. L.; Jernigan, G. G.; Culbertson, J. C.; Hite, J. K.; Yang, Y.; Daniels, K. M.; Myers-Ward, R. L.; Eddy, C. R.; Robinson, J. A.; Trumbull; *et al*. Morphology Characterization of Argon-Mediated Epitaxial Graphene on C-face SiC. *Appl. Phys. Lett.* **2010**, *96*, 2221031–2221033.
25. Emtsev, K. V.; Speck, F.; Seyller, T.; Ley, L.; Riley, J. D. Interaction, Growth, and Ordering of Epitaxial Graphene on SiC{0001} Surfaces: A Comparative Photoelectron Spectroscopy Study. *Phys. Rev. B* **2008**, *77*, 155303-1–155303-10.
26. Maruyama, B.; Ohuchi, F. S.; Rabenberg, L. Chemical Interactions in the Al−C and Al−Si−C Systems. *Mater. Res. Soc. Symp. Proc.* **1990**, *170*, 167–172.
27. Maruyama, B.; Ohuchi, F. S. H_2O Catalysis of Aluminum Carbide Formation in the Al−Si−C System. *J. Mater. Res.* **1991**, *6*, 1131–1134.
28. Nguyen, D.; Hogan, K.; Blew, A.; Cordes, M. Improved Process Control, Lowered Costs and Reduced Risks Through the Use of Nondestructive Mobility and Sheet Carrier Density Measurements on GaAs and GaN Wafers. *J. Cryst. Growth* **2004**, *272*, 59–64.
29. Novoselov, K. S.; Geim, A. K.; Morozov, S. V.; Jiang, D.; Katsnelson, M. I.; Grigorieva, I. V.; Dubonos, S. V.; Firsov, A. A. Two-Dimensional Gas of Massless Dirac Fermions in Graphene. *Nature* **2005**, *438*, 197–200.

30. Zhang, Y. B.; Tan, Y. W.; Stormer, H. L.; Kim, P. Experimental Observation of the Quantum Hall Effect and Berry's Phase in Graphene. *Nature* **2005**, *438*, 201–204.
31. Robinson, J. A.; LaBella, M.; Trumbull, K. A.; Weng, X. J.; Cavelero, R.; Daniels, T.; Hughes, Z.; Hollander, M.; Fanton, M.; Snyder, D. Epitaxial Graphene Materials Integration: Effects of Dielectric Overlayers on Structural and Electronic Properties. *ACS Nano* **2010**, *4*, 2667–2672.
32. Moon, J. S.; Curtis, D.; Bui, S.; Marshall, T.; Wheeler, D.; Valles, I.; Kim, S.; Wang, E.; Weng, X.; Fanton, M. Top-Gated Graphene Field-Effect Transistors Using Graphene on Si (111) Wafers. *IEEE Elect. Dev. Lett.* **2010**, *31*, 1193–1195.
33. Reina, A.; Jia, X. T.; Ho, J.; Nezich, D.; Son, H. B.; Bulovic, V.; Dresselhaus, M. S.; Kong, J. Large Area, Few-Layer Graphene Films on Arbitrary Substrates by Chemical Vapor Deposition. *Nano Lett.* **2009**, *9*, 30–35.
34. Kedzierski, J.; Pei-Lan, H.; Reina, A.; Jing, K.; Healey, P.; Wyatt, P.; Keast, C. Graphene-on-Insulator Transistors Made Using C on Ni Chemical-Vapor Deposition. *IEEE Elec. Dev. Lett.* **2009**, *30*, 745–747.
35. Robinson, J. A.; LaBella, M.; Zhu, M.; Hollander, M.; Kasarda, R.; Hughes, Z.; Trumbull, K.; Cavalero, R.; Snyder, D. Contacting Graphene. *Appl. Phys. Lett.* **2011**, *98*, 053103-1–53103-3.
36. Graf, D.; Molitor, F.; Ensslin, K.; Stampfer, C.; Jungen, A.; Hierold, C.; Wirtz, L. Spatially Resolved Raman Spectroscopy of Single- and Few-Layer Graphene. *Nano Lett.* **2007**, *7*, 238–242.